

**Numerical and Experimental Investigations on Mechanical Stress
in 3D Stacked Integrated Circuits for Imaging Applications**

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Abstract: Pursuing the trend towards miniaturization and increased performance of integrated circuits, new processes and architectures are constantly developed. In this thesis, we are interested in emerging assembly processes applied to specific products. On the one hand, 3D integrated circuits are becoming an increasingly viable approach to enable continuous downscaling, instead of conventional planar integration. On the other hand, to improve the performance of CMOS image sensors, in recent years the backside-illumination approach was developed, involving specific integration and operation requirements. An innovative approach consists in the vertical stacking of such image sensors on a more advanced logic circuit using direct bonding of hybrid metal/oxide surfaces. This work investigates thermomechanical stress build-up during fabrication processes for these emerging architectures.

Keywords: *CMOS Image Sensors - Hybrid Bonding - Wire Bonding – Piezoresistive Stress Sensors - Finite Element Modeling*